COMPRESSED IMAGE AUDIO DECODER

Publication number: JP9307865

Publication date: 1997-11-28

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Applicant: HITACHI LTD

Classification:

- international: ***H04N7/26; H04N7/08; H04N7/081; H04N7/24;*** **H04N7/26; H04N7/08; H04N7/081; H04N7/24;** (IPC1-7): H04N7/08; H04N7/081; H04N7/24

- European:

Application number: JP19960120244 19960515

Priority number(s): JP19960120244 19960515

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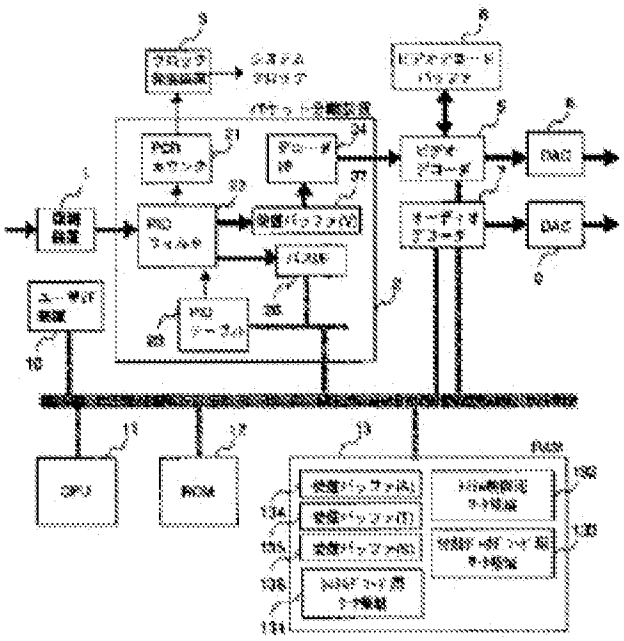
Abstract of **JP9307865**

PROBLEM TO BE SOLVED: To ensure an operation margin of a CPU by providing a reception buffer with respect to other packets than image data into a memory RAM of the CPU and providing a reception buffer for an image packet into a packet separator, and to omit a memory exclusively for a data buffer. SOLUTION: An image packet is fed to an exclusive reception buffer 27 and data are transferred via a decoder interface 24 on request of a video decoder 5. Furthermore, an audio packet reception buffer 134, an additional data packet reception buffer 135 or the like are provided in the inside of a RAM 13 in addition to a system decoding work area 131 or the like and packets other than the image are transferred to a packet reception buffer to each element via a bus interface 26. A CPU 11 reads transport stream packets stored in each reception buffer in the order of arrival according to a control program stored in a ROM 12 and conducts the processing to each element.



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